What is claimed is:

1. A method of fabricating a vertical metal-insulator-metal capacitor (MIMCap), comprising:

providing a wafer having a workpiece;

depositing an insulating layer over the workpiece;

patterning the insulating layer with a plurality of trenches, the insulating layer comprising at least one first region and at least one second region, the first region comprising trenches for at least one MIMCap;

depositing a first conductive layer over the insulating layer within the trenches;

depositing a resist over the insulating layer first regions;

depositing a second conductive material within the insulating layer second region trenches;

removing the resist;

depositing a thin dielectric layer over the insulating layer second region within the second region trenches; and

depositing a third conductive material over the thin dielectric layer within the second region trenches.

2. The method according to Claim 1, further comprising chemically-mechanically polishing the surface of the wafer to remove the first conductive layer, second conductive material, thin dielectric layer, and third conductive material from the top surface of the insulating layer, leaving at least one vertical MIMCap in the insulating layer first region.

3. The method according to Claim 2, wherein a plurality of vertical MIMCap's are formed in the insulating layer first region, further comprising coupling at least two of the vertical MIMCap's together.

4. The method according to Claim 2, wherein the CMP simultaneously forms MIMCap's in the insulating material first region and conductive wiring in the insulating material second region.

5. The method according to Claim 1, wherein depositing the first conductive layer comprises depositing a conductive liner.

6. The method according to Claim 5, wherein depositing the first conductive layer comprises forming a conductive seed layer over the conductive liner.

7. The method according to Claim 6, wherein the conductive liner and conductive seed layer comprise at least one MIMCap bottom plate.

8. The method according to Claim 6, wherein depositing the conductive liner comprises depositing TaN, Ta, TiN or combinations thereof by chemical vapor deposition (CVD) or physical conductive vapor deposition (PVD), wherein forming the conductive seed layer comprises depositing a copper seed layer by PVD or CVD.

9. The method according to Claim 1, wherein depositing the second conductive layer comprises depositing copper by electroplating or physical vapor deposition (PVD), wherein depositing the third conductive material comprises depositing W, TiN, Al, Ta, Ti, TaN, TiW, Cu, Si, or combinations thereof by physical vapor deposition (PVD) or chemical vapor deposition (CVD), wherein the third conductive material forms the MIMCap top plate.

10. The method according to Claim 1, wherein depositing the thin dielectric layer comprises depositing a conformal dielectric having a thickness of 10 nm to 200 nm.

11. The method according to Claim 10, wherein depositing the thin dielectric layer comprises depositing silicon nitride, Ta_2O_5, or combinations thereof by plasma-enhanced chemical vapor deposition (PECVD).

12. A method of fabricating a vertical metal-insulator-metal capacitor (MIMCap), comprising:

providing a wafer having a workpiece;

depositing an inter-level dielectric over the workpiece;

patterning the inter-level dielectric with a plurality of trenches, the inter-level dielectric comprising at least one first region and at least one second region, the first region comprising trenches for at least one MIMCap, the second region comprising trenches for a plurality of conductive lines;

depositing a conductive liner over the inter-level dielectric within the trenches;

depositing a seed layer over the conductive liner;

depositing a resist over the conductive liner;

removing the resist over the conductive liner in the inter-level dielectric second regions, leaving resist over the conductive liner in the inter-level dielectric first regions;

depositing a first conductive material within the insulating layer second region trenches to form a plurality of conductive lines;

removing the resist;

depositing a MIMCap dielectric over the inter-level dielectric second region within the second region trenches; and

depositing a second conductive material over the MIMCap dielectric within the second region trenches to form a MIMCap top plate.

13. The method according to Claim 12, further comprising chemically-mechanically polishing (CMP) the top surface of the wafer to remove the conductive liner, seed layer, first conductive material, MIMCap dielectric, and second conductive material from the top surface of the inter-level dielectric, leaving at least one vertical MIMCap in the insulating layer first region.

14. The method according to Claim 13, wherein a plurality of vertical MIMCap's are formed in the inter-level dielectric first region, further comprising coupling at least two of the vertical MIMCap's together.

15. The method according to Claim 13, wherein the CMP simultaneously forms at least one MIMCap in the inter-level dielectric first region and the plurality of conductive lines in the inter-level dielectric second region.

16. The method according to Claim 12, wherein the conductive liner and conductive seed layer comprise at least one MIMCap bottom plate.

17. The method according to Claim 12, wherein depositing the conductive liner comprises depositing TaN, Ta, TiN or combinations thereof by chemical vapor deposition (CVD) or physical conductive vapor deposition (PVD), wherein forming the conductive seed layer comprises depositing a copper seed layer by PVD or CVD.

18. The method according to Claim 12, wherein depositing the first conductive layer comprises depositing copper by electroplating or physical vapor deposition (PVD), wherein depositing the second conductive material comprises depositing W, TiN, Al, Ta, Ti, TaN, TiW, Cu, Si, or combinations thereof by physical vapor deposition (PVD) or chemical vapor deposition (CVD).

19. The method according to Claim 12, wherein depositing the MIMCap dielectric comprises depositing a conformal dielectric having a thickness of approximately 10 nm to 200 nm.

20. The method according to Claim 19, wherein depositing the MIMCap dielectric comprises depositing silicon nitride, Ta_2O_5, or combinations thereof by plasma-enhanced chemical vapor deposition (PECVD).